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10/764,003	01/22/2004	Ramin Farjad-rad	3003P	8941

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EXAMINER	
FOTAKIS, ARISTOCRATIS	
ART UNIT	**PAPER NUMBER**
2611	
MAIL DATE	**DELIVERY MODE**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,003	FARJAD-RAD, RAMIN	
	Examiner	Art Unit	
	Aristocratis Fotakis	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/15/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5 - 10, 12- 16 and 18 - 23* is/are rejected.

7)☒ Claim(s) *4, 11 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/15/2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a) because they fail to show pointers on how the signals are directed in figures 3 and 4 as described in the specification. It is not clear how the signal is directed between the two summers 106a and 106b. The drawings were amended to show pointers on the direction of the clock signals. However, as observed, this cannot be correct. It seems the clock signals are pointed in the opposite direction. For example, the last phase detector has three inputs (ck3, ck0 and pd3) without an output, where the input pd3 should be an output from the phase detector. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the

remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 8 is objected to because of the following informalities: Line 3 of the claim recites of "plurality of docks". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 2, 8 - 9, 15, 19 - 20 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al (US PG-Pub 2002/0085656).

Re claims 1, 15, 19 - 20 Lee teaches of a phase offset cancellation circuitry (Fig.4) comprising: at least two phase detectors (#407, Fig.5) for receiving component clock signals of a multi-phase clock generator (CLK 1 to 3, Figs.5 and 8), wherein at least some of the clock signals are offset from each other (variable delay, Fig.8 and Phase shifter, Figs.7 and 4), each of the at least two phase detectors for detecting phase differences between pairs of component clock signals (PD1 and PD2, Fig.5); at least one summer (#601, phase estimator, Fig.6) coupled to the at least two phase detectors for measuring the phase differences between the at least two phase detectors (#603, Fig.6); and at least one variable delay element (#801, Fig.8 or #707, Fig.7) for receiving the measured phase differences (#411, Figs.7 and 8 from phase controller) and for providing a delay which is proportional to an output value of the at least one summer (#601), wherein the delay is used to reduce the phase difference between pairs of component clock signals (CLK 1 to 3, Fig.8 or Fig.7) (Paragraphs 0030 - 0036).

Re claims 2 and 9, Lee teaches of each of the at least two phase detectors measures a phase spacing (phase error) of adjacent component clock signals (#404 and #405 or #405 and #406).

Re claims 8 and 22, Lee teaches of a multi-phase clock generator (#413, Fig.4) comprising: a plurality of clocks for clocking input data (CLK 1 to 3); a plurality of samplers coupled to the plurality of clocks for receiving the input data (Data sampler,

#403, Fig.4) each of the samplers receiving a different clock phase (from phase shifter); and a phase offset cancellation system coupled to the plurality of clocks (#407, #410, Figs 5 - 6), the phase offset cancellation system further comprising a plurality of phase detectors for receiving component clock signals of the multi-phase clock generator (COMPARE LOGIC, #407), wherein at least some of the clock signals are offset from each other (phase shifted), each of the plurality of phase detectors for detecting phase differences between pairs of component clock signals (#404 and #405 or #405 and #406); at least one summer coupled to the two phase detectors for measuring the phase differences between the at least two phase detectors; and at least one variable delay element for receiving the measured phase differences and for providing a delay which is proportional to an output value of the at least one summer, wherein the delay is used to reduce the phase difference between pairs of component clock signals (see rejection of claim 1 above).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3, 5 – 7, 10, 12 – 14, 16, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Dally et al (US 6,275,072)

Re claims 3, 10 and 16, Lee teaches all the limitations of claims 1 except of specifically teaching of wherein each of the at least two phase detectors comprise: a current source; and two switches coupled to the current source, the two switches receiving a first and a second component clock signal, wherein when the two switches are closed the phase detector generates an indication of the difference between the first and second clock signals.

Dally teaches of a phase comparison of timing signals made by combinational circuitry which receives the timing signals and a window signal, the window signal identifying edges of the timing signals to be compared. The comparison may result in a charge pumped output which can be fed back to control the phase of one of the timing signals. The phase comparator and charge pump circuit can be included in a multiplier circuitry in which the phase of an input signal is directly compared to the phase of an

edge of the multiplied signal (Abstract). Dally teaches of phase detection comprising a current source; and two switches coupled to the current source, the two switches receiving a first and a second component clock signal, wherein when the two switches are closed the phase detector generates an indication of the difference between the first and second clock signals (Fig.10, Col 6, Lines 42 – 67).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the mirror circuit of Dally which includes the current source and the two switches for receiving a first and second clock signal so as to reliably compare the two signals.

Re claims 5 – 6 and 12 - 13, Lee teaches all the limitations of claims 1 except of each of the at least two phase detectors provides a voltage or a current as an output.

Dally teaches of the phase detection circuitry providing either a voltage or a current as an output.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have provided a voltage signal or a current signal as an output where the current is proportional to the voltage.

Re claims 7, 14 and 18, Lee teaches all the limitations of claims 1 except of the at least two phase detectors are calibrated to minimize device mismatch within the phase detector.

Dally teaches of the phase detection circuitry that solves the problems of phase offset due to gate mismatch (Col 4, Lines 51 – 67).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have calibrated the phase detector in order to minimize device mismatch.

Claims 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Casper (US 6978012).

Lee teaches of a system comprising: a multi-phase clock generator; phase offset cancellation circuitry for cancelling phase offsets of the multi-phase clock generator, the phase offset cancellation circuitry being coupled to the multi-phase clock generator, the phase offset cancellation circuitry further comprising at least two phase detectors for receiving component clock signals of a multi-phase clock generator, wherein at least some of the clock signals are offset from each other, each of the phase detectors for detecting phase differences between pairs of component clock signals; at least one summer coupled to the two phase detectors for measuring the phase differences between the at least two phase detectors; and at least one variable delay element for receiving the measured phase differences and for providing a delay which is

proportional to an output value of the at least one summer, wherein the delay is used to reduce the phase difference between pairs of component clock signals (see rejection of claim 1). However, Lee does not teach of a driver that is clocked by the phase offset cancelled multi-phase clock generator in a transmitter.

Casper teaches of an echo cancellation technique that can be applied to a transmission line signal received by an input/output (i.e., I/O) circuit of an integrated circuit device (Col 1, Lines 29 – 33) where the sampler unit (#224, Fig.2) is clocked by the receiver clock signal that may be phase and frequency locked to the driver clock signal (Col 6, Lines 12 – 35, Fig.2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have applied the data sampling system of Lee to the system of Casper where sampler unit is clocked by the receiver clock signal that may be phase and frequency locked to the driver (transmitter) clock signal so that the receiver and the transmitter are synchronous.

Allowable Subject Matter

Claims 4, 11 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristocratis Fotakis whose telephone number is (571) 270-1206. The examiner can normally be reached on Monday - Thursday 6:30 - 4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AF

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER